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ANALYTICAL MODELING AND SIMULATION OF A 7NM HK-MG FINFETS PERFORMANCE INVESTIGATION IN TERMS OF IMPROVED SENSITIVITY FOR TEMPERATURE NANOSENSING APPLICATIONS

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Abstract

Within the realm of contemporary microelectronics, the Fin-shaped Field Effect Transistor (FinFET) serves as a major competitor. By virtue of its one-of-a-kind structure, it is possible to scale the device down to the sub-nanometer domain and to imitate the electrical properties of a MOSFET thereby achieving reduce SCEs and improved performance. Using gallium arsenide (GaAs) as the metal gate (MG) and lanthanum aluminum oxide ($LaAlO_3$) as the high-k (HK) dielectric material, this study offers an analytical model of drain to source current (Ids) for a FinFET at 7nm Technology node. Electrical parameters are examined by solving three-dimensional (3-D) Poisson's equation using continuity equations. Validation of the resulting analytical model is performed using 7nm FinFET simulations using HK-MG approach. All of the aforementioned models are subjected to temperature changes ranging from 275k to 450k in order to explore the influence that HK-MG gate dielectrics have on short channel effects (SCEs). The analytical model and the results of the simulations that resulted are used to calculate the temperature sensitivity (S_T(max) = 22mV/kelvin) and the temperature coefficient of resistance (TCR max = 3.3 mppm/kelvin).

Index Terms: *Poisons Distribution, Continuity Equations, Temperature Sensitivity, Temperature Coefficient of Resistance, Short Channel Effects.*

1. INTRODUCTION

Due to the negative impact of downscaling on device performance, especially in low-power applications, the semiconductor industry is exploring new alternatives to Metal Oxide Semiconductor Field Effect Transistors (MOSFET) in an effort to enhance device performance. To achieve low power consumption and high-speed performance, semiconductor devices are transitioning from the micro to the nano scale. This change leads to a decrease in the ON-state current (I_{ON}), resulting in a decline in performance. Moreover, when the gate is in the off-mode, it fails to completely deactivate the channel, resulting in a rise in the current flow (I_{OFF}) between the drain and the source [1], [2]. Scalability affects the cost, density, speed, functionality and power dissipation of an integrated circuit (IC). To enhance gate control over the channel and improve electrostatic behavior, the scaling of transistors requires the implementation of a multi-gate transistor structure. Due to continued downscaling, MOSFETs have now reached their practical limits, leading to a decline in their original properties due to short channel effects (SCEs) [3]–[5]. Upon activation of the SCEs, the device encounters heightened power dissipation and alterations in the process. The SCEs often occur due to the strong electric field

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lines extending from the drain to the source area, along with the potential for closely spaced source/drain to body depletion zones across the channel to make contact with each other due to the punch-through problem [6]–[8].

One of the semiconductor devices suggested to tackle these problems were double-gate (DG) FETs, which are being viewed as possible replacements for MOSFETs. There are several benefits associated with the independent gate DG-MOSFET. For example, it enables the modification of the threshold voltage using back gate bias, as well as the creation of both analog and digital circuits. One potential concern that may arise with DG-FETs is the misalignment of the gates. This paved the way for the use of Trigate FETS (TG-FETs) which can optimize the performance of DG-FETs and enhance electrical parameter behavior [9]–[11]. However, by utilizing three distinct gates, there is a possibility that the misalignment could result in overlap capacitance and source/drain resistance. Despite providing improved control compared to planar transistors, Tri-gate FETs encounter challenges in effectively suppressing SCEs at very small geometries. The shift from tri-gate Field-Effect Transistors (FETs) to FinFETs was mainly motivated by the necessity to address certain constraints linked to tri-gate FETs, especially as devices were being scaled down. As a three-dimensional asymmetrical structure, the FinFET has been subject to different shape adjustments to boost SCEs and enhance device operation. Extra structures like the surrounding gate, omega-shaped gate, and pi-shaped FinFETs are included for analyzing and enhancing the performance of the electrical characteristics. Through the removal of the parasitic electric field lines originating from the source and drain, the FinFET boosts the channel's resistance to SCEs. This device demonstrates an increased drive current while maintaining a consistent I_{OFF}. FinFET provides several benefits including high current drive, efficient use of space and precise electrostatic gate control [12]–[14].

Furthermore, a blend of different materials in FinFET architectures is introduced to improve the device's performance. Researchers have noted that incorporating low band gap materials and high dielectric constant (HK) materials like germanium (Ge), gallium arsenide (GaAs), and gallium nitride (GaN) in the channel leads to high I_{ON} / I_{OFF} and minimal SCEs. This is primarily due to the significantly higher mobility of these materials when compared to silicon (Si) [15]–[18]. By enhancing the gate-channel capacitance through thinner gate oxides and HK dielectric materials, this issue can be somewhat alleviated. Several high dielectric constant materials have been proposed to reduce leakage current and preserve the High-K value. The materials listed are Al_2O_3 (k = 9), Y_2O_3 (k = 15), and HfO_2/ZrO_2 (k = 25). It is because GaAs/GaN based FinFETs exhibit superior electrical performance compared to elemental FinFETs. Lately, there have been some promising advancements. For mobility, saturation velocity, and breakdown voltages, GaN based metal gate (MG) devices offer exceptional performance. Moreover, the generation of a two-dimensional electron gas (2DEG) at the AlGaN/GaN interface leads to a larger electron density, enabling higher currents to be achieved at the same bias level. This is due to the wider bandgap and the application of the piezoelectric effect. Moreover, when compared to Si, GaAs shows a reduced intrinsic carrier concentration at elevated temperatures [17], [19]–[21].

Temperature variations impact the electrical characteristics of the FinFET, particularly the current flow, allowing for accurate temperature measurements. Studies have delved into the impact of temperature on FinFET transistors to assess their viability as nano-temperature sensors [22]–[27]. Through simulations of the I-V characteristics of FinFETs at various temperatures, researchers discovered that specific FinFET configurations, like those utilizing Gallium Arsenide (GaAs) or Silicon (Si), demonstrate notable variations in their electrical performance in response to temperature changes. Such sensitivity enables the creation of extremely accurate nano-sensors for measuring temperature [20], [28]–[30]. A more intricate design incorporates a blend of temperature and voltage sensors created using FinFET technology. This design has the capability to convert the voltage across

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a resistor into an output clock, allowing for precise temperature measurements. These sensors have been created using cutting-edge FinFET processes, highlighting the technology's capacity to offer precise temperature sensing with low power usage and a small footprint. The compact size and efficient energy usage of FinFET-based temperature sensors are ideal for dense thermal sensing in microprocessors. An illustration showcases a current-controlled oscillator (CCO) sensor that is extremely compact and energy-efficient, making it well-suited for on-die thermal sensing to regulate power and performance aspects in intricate ICs.

Utilizing a mathematical model to explain the properties of the device, such as channeled and physical factors, is seen as a valuable approach to optimize the device's potential applications. Researchers have been studying modeling and experimental investigations of FinFETs, with a focus on the importance of physics-based models of these devices in the field of information technology. An in-depth analysis of a device reveals that its behavior aligns with all the variables present within the device and its operation. Modeling semiconductor devices starts by examining the basic electrical properties found within the channel of the device [31]–[34]. These parameters encompass energy bandgap, electron density, surface potential, electric field, and various other factors. There are numerous methods available to address the surface potential of the device. One can obtain explanations through closed-form expressions with the help of these models, which do not require extensive iterations like those in industrial simulators. These models are well-suited for predicting the parameters of circuit-based applications because of their accuracy and reliability, making them suitable for this task. Furthermore, to optimize the utilization of a device within a VLSI circuit, it is crucial to have analytical models that are suitable and efficient. Several research studies have been detailed in the literature regarding DG MOSFET on two-dimensional (2D) analysis. These studies have been conducted using simulations and analytical techniques. Researchers have developed models for conduction charge and drain current of n+-p+ double gate SOI MOSFETs. In addition, the researchers have explored an analytical physically based model for undoped FinFET devices, incorporating the mobile charge term, in both the subthreshold and near-threshold regions. The comparison was made between the analytical expression of subthreshold features and the parameters of the SCEs, which involved subthreshold slope, roll-off, subthreshold current, and DIBL, in addition to experimental data that was obtained with reasonable compromises [35]–[43].

This paper discusses the validation of the simulated drain to source current and temperature sensitivity by utilizing the 3-D Poisson’s equation. An analytical model of Ids is established based on the minimum surface potential position from the 3-D Poisson’s equation. An analytical expression for S of the transistor is also obtained from Poisson’s equation. The results illustrated theoretically are compared with data from numerical simulations and it was observed that they are in good alignment. Moreover, an analysis has been conducted on the influence of the HK-MG pair on SCEs.

2. SIMULATION MODEL

A 7nm FinFET-based temperature nano-sensor is seen in the figure-1. This nano-sensor makes use of the temperature-dependent features of materials in order to detect fluctuations in temperature on a nanoscale. This includes different parameters such as gate length (also known as channel length), fin width (also referred to as channel width or fin thickness), and other relevant features shown in Table-1. Temperature sensors using transistors are developed based on the temperature properties of current-voltage curves of the transistor. One can utilize the transistor in FET device structures as a temperature sensor by linking the gate with either the source or drain. Temperature sensors based on FinFET technology leverage the temperature-sensitive electrical properties of FinFET devices for temperature measurement. One common method is to create a circuit that produces a voltage or current signal corresponding to the absolute temperature.

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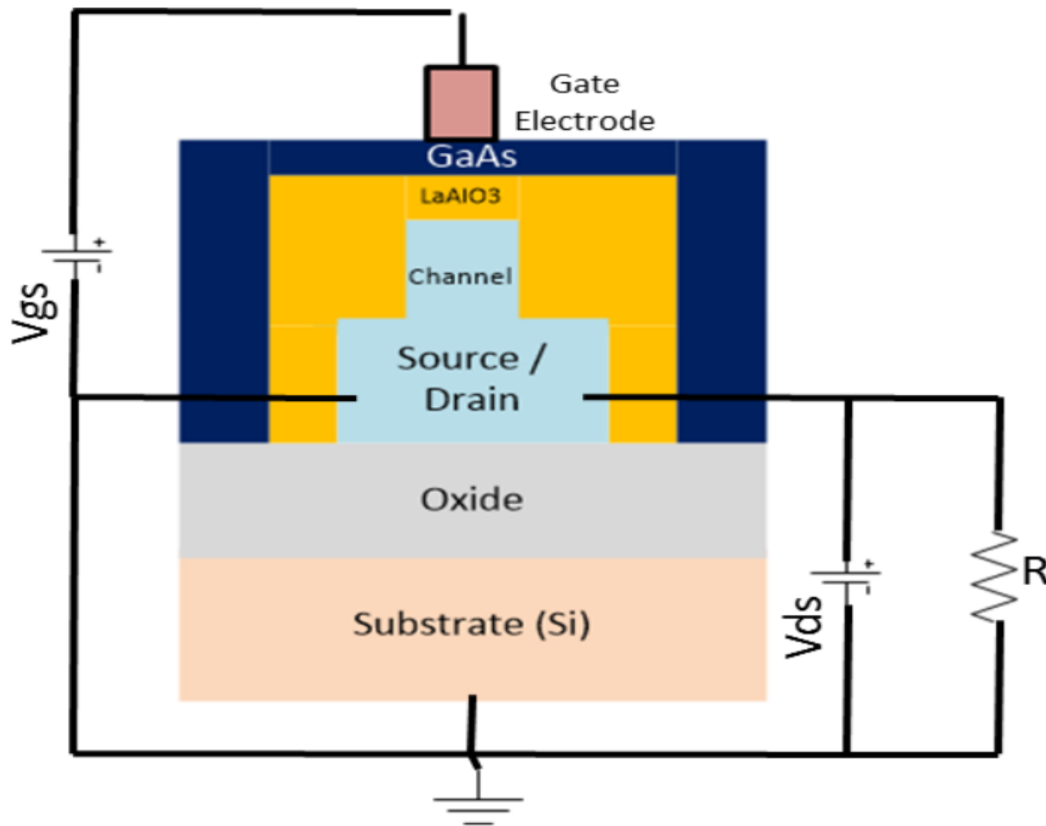

Figure 1: FinFET device circuitry for Temperature Nanosensing Application

The substrate layer of the device, which is commonly silicon, serves as a basis for the building of the FinFET structure. An electrical isolation of the device is achieved with the assistance of the insulating layer, which also helps to prevent any leakage current that may pass straight to the substrate. The source and drain of a FinFET are often raised structures that resemble fins, which is where the name that the device gets its name from. An extremely thin structure that resembles a fin, the metal gate channel is constructed out of gallium arsenide (GaAs), which is a compound semiconductor that has a high electron mobility. Whenever a voltage is supplied to the gate electrode, the area that is referred to as the channel is the one through which carriers flow. There is a thin layer of high-k dielectric material ($LaAlO_3$) that separates the gate electrode from the channel. The gate electrode is located on top of the channel. This "HK" refers to the high dielectric constant, which enables the gate to efficiently regulate the flow of carriers in the channel without the need for a thick layer. As a result, the scaling features of the device are maintained. For the purpose of determining the operating voltage by using the measured drain to source current, the resistor is a component of the external circuit and is linked to the drain of the FinFET.

Due to the fact that the carrier mobility and the threshold voltage of the FinFET are both dependent on temperature, the current that flows through the channel of the FinFET (I_{ds}) varies with temperature when the device is functioning as a temperature sensor. Because the carrier mobility in GaAs normally decreases with increasing temperature, the current would drop for a given V_{gs}, if the temperature were to rise. On the other hand, the threshold voltage could shift depending on the temperature, which might have a more complicated impact on the current. It is possible to determine the change in I_{ds} by either measuring the voltage drop across the resistor (by using Ohm's equation V = IR) or by measuring the current directly with a current meter. For temperature sensors, the output voltage is

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proportional to the temperature measured [44]. The contact resistance would typically be characterized by measuring the voltage drop across a contact at a known current. The biasing condition often referred to as a current-driven control mechanism in a sensing circuit is considered to be at 50µA to undergo required sensing by the electrodes. There is a correlation between the change in current or voltage and the change in temperature, and this particular change may be calibrated to offer an accurate readout of the temperature. The sensitivity of the sensor, which is defined as the amount by which the current varies in response to a change in temperature, is contingent upon the material characteristics of the GaAs channel and the $LaAlO_3$ oxide dielectric, in addition to the dimensions of the FinFET, which include the width, length, and height of the components. It is possible for this sort of sensor to offer extremely localized temperature data because of the nano-scale dimensions of the FinFET. This form of sensor is useful in applications where thermal management at the micro or nano-scale is essential, such as in integrated circuits and microprocessors [45].

Table 1: 7nm FinFET Device parameters

Parameter	Value
Channel Length (L_g)	15nm
Channel Width (W_{ch})	7nm
Channel Height (H)	18nm
Oxide Thickness or thickness of the fin (t_{ox} / t_{fin})	6.5nm
Source or Drain Length (L_s or L_d)	2nm
Source or Drain Overlap to Gate (O_s or O_d)	0.2nnm
Source or Drain Doping concentration	3.00E+26 cm-3
Channel Doping	2.86.00E+25 cm-3
Gate Voltage (V_{gs})	0.7V
Temperature (in Kelvin)	275k to 450k
Drain Voltage (V_{ds})	0.01 – 0.69V
HK Oxide Material	Lanthanum Aluminum Oxide ($LaAlO_3$)
Metal Gate Material	Gallium Arsenide (GaAs)
Resitor (R)	V_{gs} / 50µA

3. ANALYTICAL MODEL

Exploring the static and dynamic properties of a semiconductor device when exposed to external fields, indeed, involve complex interactions that can be mathematically described by a set of coupled differential equations. One of these crucial equations is the Poisson's equation, which relates the electrostatic potential (φ) to the charge density and charge density (ρ) within the semiconductor.

The standard form of Poisson's equation for electrostatic potential Φ in a semiconductor material is given by equation (1)

$$\nabla^2\Phi = -\frac{\rho}{\varepsilon} = -\frac{\rho}{k\varepsilon_0} \quad (1)$$

Where, ∇^2 is the Laplacian operator, representing the divergence of the gradient of a field, in this case, the electrostatic potential Φ. ρ is the charge density within the semiconductor and ε=-$k\varepsilon_0$. Where, k is the dielectric constant.

To derive an expression of Drain to Source Current (I_{ds}), sequences of assumptions are to be made as follows:

Assumption-1**:** It is fair to assume that only minority carriers are responsible for Ids; for example, in a FinFET device, the hole current may be ignored. The number of minority carriers in inversion much outnumbers the number of majority carriers since the fin is either not doped at all or very minimally

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doped. The bulk of carrier holes in FinFETs result from impact ionization. These faults become critical when attempting to describe the device's functions when in avalanche mode. However, the Ids does not account for the breakdown regime seen in the typical working range of FinFET devices. As a result, under normal biasing conditions, the assumption that the current in FinFETs is caused by minority carriers is valid. Thus, while calculating drain current for FinFET devices, we simply consider the minority carrier current density (J_n) [46].

***Assumption-2*:** In the context of semiconductor physics, particularly when discussing the behavior of devices like n-type FinFETs under static conditions and assuming no generation (G_n) and recombination (R_n) of carriers, the continuity equation simplifies significantly. The given scenario describes such a case, leading to a simplified form of the continuity equation for electron current density (J_n). The general form of the continuity equation for electrons, considering the rate of change of charge, generation, and recombination, is given by equation (2). When there is no generation or recombination of carriers within the semiconductor device, the equation (2) results in zero [46].

$$\nabla . J_n = q(R_n - G_n) = 0 \qquad (2)$$

Where, J_n is the electron current density vector, R_n is the recombination rate of electrons, G_n is the generation rate of electrons and q is the elementary charge.

This simplification has significant implications for an nFinFET device under static conditions: The total drain current (I_{ds}) is constant at any point along the channel of the device. This means that, despite the complex three-dimensional structure of a FinFET, under these assumptions, the current does not vary along the length of the channel. The conservation of current density and the assumption of no carrier generation or recombination simplify the analysis of the device's static behavior. It allows for more straightforward calculations of the device's electrical characteristics under a given set of conditions. This property is useful for understanding the device's operation in the linear (ohmic) region and saturation region, facilitating the design and analysis of circuits that incorporate FinFETs.

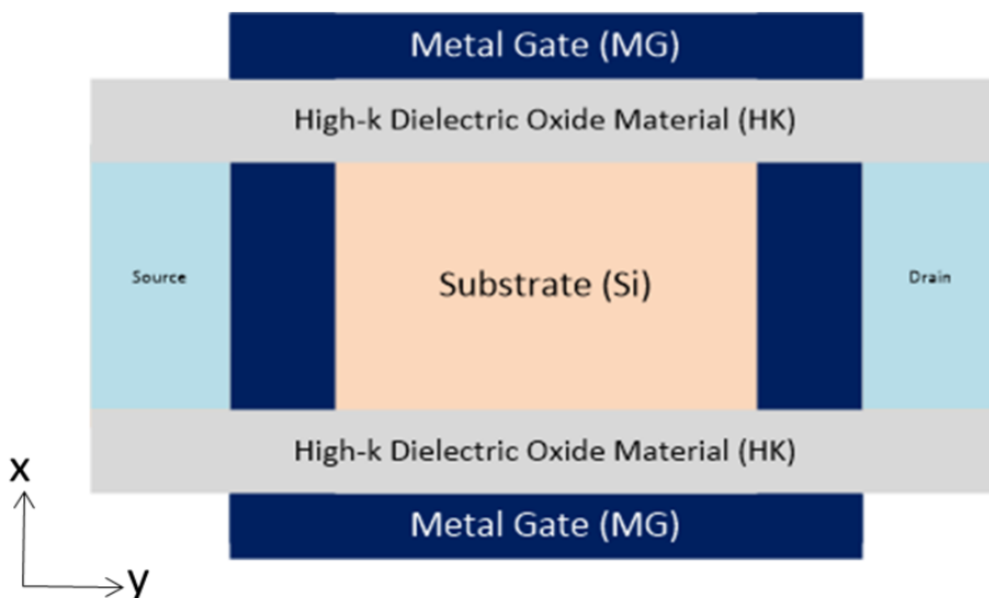

Figure 2: Cross sectional view of FinFET Device

***Assumption-3*:** The Figure-2 outlines a cross-sectional view of an n-type FinFET, where the current flows only in the y-direction, and the electron quasi-Fermi potential (Φ_n) remains constant in the x-

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direction. This simplification leads to a specific form of the equation for the electron current density ($J_n(y)$) expressed in equation (3) and how it relates to the total drain current (I_{ds}) expressed in equation (4) in the device [46].

$$J_n(y) = -qn(x,y)\mu_s(x,y)\frac{\partial \Phi_n}{\partial y} \tag{3}$$

Where, μ_s is the surface mobility and n is the electron concentration.

The assumption that $\frac{\partial \Phi_n}{\partial x} = 0$, implies that the electron quasi-Fermi level does not vary in the x-direction, focusing the analysis on variations along the channel length (y-direction). By integrating the current density $J_n(y)$ throughout the cross-sectional area of the channel, which is the product of the channel width W and the channel length 'L', it is then possible to compute the total drain current (I_{ds}) at any point 'y' along the channel. This may be done at any point along the channel.

Assuming once again that the generalized algebraic equation is valid over the whole length of the channel, we are able to get the formula for I_{ds} by integrating Equation (3) along the channel length, beginning at y = 0 and ending at y = L [46].

$$I_{ds} = \frac{W}{L}\mu_s\int_0^{V_{ds}} Q_i(y)\, dV_{ch}(y) \tag{4}$$

The expression in equation (5) represents the energy band gap of Gallium Arsenide (GaAs) material as a function of temperature (T in Kelvin) [47].

$$E_g = 1.519 - \frac{5.405\, T^2 * 10^{-4}}{T+204} \tag{5}$$

The energy band gap decreases with increasing temperature, a behavior that is common to many semiconductor materials. The specific coefficients and terms in this formula are empirical, derived from experimental data to accurately model the behavior of GaAs over a range of temperatures. The first term, 1.519 eV, represents the band gap energy at absolute zero temperature. The second term accounts for the decrease in band gap energy with increasing temperature, which attributes to the lattice expansion and electron-phonon interactions as the temperature increases. The temperature-dependent behavior of the band gap is crucial for understanding and predicting the performance of semiconductor devices made from GaAs, especially in applications sensitive to changes in temperature, such as temperature nanosensors.

The effective density of states in the valence band (N_v) and in the conduction band (N_c) are critical parameters in semiconductor physics, as they influence the carrier concentration and the behavior of semiconductor devices under various conditions [48].

The effective density of states in the Conduction band is given by equation (6):

$$N_c = 8.63T^{1.5} * 10^{13}[1 - 1.93\, T * 10^{-4} - 4.19T^2 * 10^{-8} + 65e^{\frac{-E_g}{2kT}}] \tag{6}$$

Where, k is the Boltzmann constant $8.617*10^{-5}$ eV/K

The first term reflects the standard temperature dependence of the effective density of states. The presence of the exponential term involving Eg, indicates the significant influence of the energy band gap's temperature dependence on the effective density of states.

The effective density of states in the Valence band is given by equation (7):

$$N_v = 1.83T^{1.5} * 10^{15} \tag{7}$$

This formula quantifies the number of available states for holes in the valence band at a given temperature. The $T^{1.5}$ dependency reflects the relationship between the temperature and the density

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of available states in the valence band, analogous to the effective density of states in the conduction band.

The intrinsic carrier concentration is a fundamental parameter in semiconductor physics, influencing the electrical properties of semiconductor materials and devices under various conditions. It is temperature-dependent, as both the thermal excitation of electrons and the effective densities of states are functions of temperature. This intrinsic carrier concentration represents the number of free electrons (or equivalently, holes) present in the semiconductor material without any external doping expressed in equation (8):

$$n_i(T) = \sqrt{N_c N_v e^{\frac{-E_g}{2kT}}} \tag{8}$$

The exponential term reflects the statistical likelihood of electrons gaining enough thermal energy to cross the band gap from the valence band to the conduction band, thus contributing to the intrinsic carrier concentration. The factor of 1/2 in the exponent signifies that, on average, an electron needs to overcome half the band gap energy to contribute to the intrinsic carrier concentration, considering the symmetry of the conduction and valence bands around the Fermi level in an intrinsic semiconductor.

The Bulk potential (Φ_B) expressed in equation (9) contributes to the creation of a depletion region around the p-n junction, where mobile charge carriers are swept away, leaving behind a region depleted of free carriers. This depletion region acts as a barrier to charge carrier movement across the junction under equilibrium conditions. The magnitude of Φ_B influences the width of the depletion region and the barrier height that carriers must overcome to move from one side of the junction to the other, affecting the diode's forward and reverse characteristics.

$$\phi_B = -\frac{kT}{q} \ln\left(\frac{N_d}{n_i(T)}\right) \tag{9}$$

Where, q is is the elementary charge which equals to $1.602*10^{-19}$C and N_d is the donor concentration, representing the density of donor atoms in an n-type which equals to 8500 cm^{-3}.

In a p-type semiconductor, where the acceptor atoms introduce holes, the hole concentration ‘p’ is approximately equal to the acceptor concentration N_a , assuming full ionization and that all acceptors contribute a hole. Under thermal equilibrium, the electron concentration ‘n’ is much lower than the hole concentration ‘p’, and it can be inferred that ‘n(X)’ is inversely proportional N_d , It ultimately results in the equation (10) that is presented for the concentration of electrons at any location x that is close to the surface of a p-type substrate.

$$n(X) = \frac{n_i^2}{N_d} \tag{10}$$

When discussing semiconductor physics, it is important to consider the impact of dopants and carriers on potential variation, which can influence device operation. This is particularly relevant in scenarios like channel formation. The Electrostatic potential in x-direction is expressed as equation (11).

$$\Phi(x) = \frac{kT}{q} \ln\left(n(X) + \frac{N_d}{n_i(T)}\right) \tag{11}$$

The logarithmic term reflects the relative increase in carrier concentration due to doping compared to the intrinsic level.

Electro-static force for moving a unit charge from 1 reference point to another separated by a distance ‘d’ is given by: $\Phi = kd$

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We solve for potential φ(x,y) in the ultrathin-body fin of FinFET devices to obtain surface potential. To solve for φ(x,y), let us consider a symmetric n-channel FinFET device. Electro-static force for moving a unit charge from one reference point 'x' to another point 'y' separated by a distance is given by equation (12).

$$\Phi(x,y) = \Phi(x) - \Phi(y) = \Phi(x) - ky = \Phi(x) - \frac{\sigma}{\varepsilon_0}y = \Phi(x) - \frac{10^6 y}{8.854} \qquad (12)$$

Where, σ is the Electrical conductivity of GaAs $=10^{-6}$ $(\Omega\text{-m})^{-1}$ and ε_0 is the relative permittivity of GaAs $= 8.854 \times 10^{-14}$ F/m

This intrinsic energy level is crucial for understanding and predicting the behavior of semiconductor devices which is expressed in equation (13) as follows:

$$E_i = \frac{E_c+E_v}{2} - \frac{kT}{q}\ln\left(\frac{N_c}{N_v}\right) \qquad (13)$$

The intrinsic energy level often reflects the midpoint between the conduction and valence band edges, adjusting for the difference in the effective densities of states in these bands, which is temperature-dependent. The subtraction of logarithmic term accounts for the fact that the effective mass (and therefore the effective density of states) of electrons and holes can be different, shifting the intrinsic level towards the band with the smaller effective mass.

According to equation (14) the electrostatic potential, denoted by the symbol φ, in a semiconductor is determined by the intrinsic Fermi level, which is denoted by the symbol E_i.

$$\Phi_i = -\frac{E_i}{q} \qquad (14)$$

The position of the electron quasi-Fermi potential (Φ_n) level relative to the conduction and valence bands influences the electrical properties of the semiconductor is expressed in equation (15), including its conductivity and behavior in electronic devices like diodes and transistors.

$$\Phi_n = \Phi_i - \frac{kT}{q}\ln\left(\frac{N_d}{n_i(T)}\right) \qquad (15)$$

The negative sign indicates that the Fermi level moves downward in energy as the donor concentration (N_d) increases, assuming that $n_i(T)$ is a constant for a given temperature and semiconductor material. This reflects the increased likelihood of finding electrons in the conduction band due to the additional donors, which ionize to provide extra electrons.

Due to the applied V_{ds}, the surface potential φ_s is a function of location y along the channel such that $\varphi_s = \varphi_s(y)$. Therefore, a channel potential $V_{ch}(y)$ exists along the channel from the source to drain such that

$$V_{ch}(y) = \begin{cases} V_{sb}; & when\ y = 0 \\ V_{sb} + V_{ds}; & when\ y = L \end{cases} \qquad (16)$$

From Equation (), $V_{ch}(0) = 0$ at the source end of the channel ($V_{sb} = 0$) and $V_{ch}(L) = V_{ds}$ at the drain end of the channel.

When operating the device, adjusting the source and drain voltages compared to the substrate causes a decrease in the quasi-Fermi level Ei (or potential φn) at the source side by qVgs, and at the drain side by (qVgs + qVds), in relation to the equilibrium Fermi level Ef in the body. The variation in φn between the source and drain causes the electrons to flow through the channel. Therefore, the channel potential Vch(y) at any given point y within the channel can be determined by equation (17).

$$V_{ch}(y) = \Phi_n(y) - \Phi_n\,(source) = ky - \Phi_n = \frac{\sigma}{\varepsilon_0}y - \Phi_n = \frac{10^6 y}{8.854} - \Phi_n \qquad (17)$$

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The minority carrier surface concentration at any point x and y is particularly useful for analyzing the behavior of minority carriers in semiconductor devices, especially in complex structures like FinFETs where electrostatic control and three-dimensional effects are crucial. Understanding minority carrier distributions is key to predicting device performance, including leakage currents, switching behavior, and overall device efficiency. This means that the quasi-Fermi potential at the surface area of a FinFET device is reduced by a certain amount, denoted as $V_{ch}(y)$, in comparison to the situation in which a MOS capacitor is present. Through the application of a factor exp(−Vch(y)/vkT), the surface electron concentration (n_s) is reduced, resulting in a decrease. After that, we can write the minority carrier surface electron concentration at any position y in the channel of a FinFET device as follows, following the derivation of minority carrier density provided by Equation (18) for a MOS capacitor is the following:

$$n(x,y) = 2.86\ 10^{25} \mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B-V_{ch}(y))q}{\mathrm{kT}}} \qquad (18)$$

The measure of total charge density is crucial for understanding and modeling the behavior of semiconductor devices, particularly in terms of how minority carriers contribute to overall device characteristics like conductivity, capacitive effects, and the modulation of channel properties in response to applied voltages which is expressed through equation (19).

$$Q_i(y) = -q\int_0^W n(x,y)dx = -qWn(x,y) \qquad (19)$$

Upon Simplification and substitution of all interrelated equations (5) to equation (19) we get;

$$I_{ds} = \frac{W}{L}\mu_s\left[\frac{2.86*10^{25}\mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B-0.69)q}{\mathrm{kT}}}}{-\frac{\mathrm{q}}{\mathrm{kT}}\mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B-0.69)q}{\mathrm{kT}}}} + \frac{\mathrm{q}*2.86*10^{25}\ \mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B)q}{\mathrm{kT}}}}{-\frac{\mathrm{q}}{\mathrm{kT}}\mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B)q}{\mathrm{kT}}}}\right] \qquad (20)$$

For simplifying the equations consider

$$\mathrm{A} = 2.86*10^{25}\mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B-0.69)q}{\mathrm{kT}}};\ \mathrm{B} = -\frac{\mathrm{q}}{\mathrm{kT}}\mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B-0.69)q}{\mathrm{kT}}};\ \mathrm{C} = \mathrm{q}*2.86*10^{25}\ \mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B)q}{\mathrm{kT}}}\ \text{and}$$

$$\mathrm{D} = -\frac{\mathrm{q}}{\mathrm{kT}}\mathrm{e}^{\frac{(\Phi(x,y)-2\phi_B)q}{\mathrm{kT}}} \qquad (21)$$

We get

$$I_{ds} = \frac{W}{L}\mu_s\left[\frac{A}{B} + \frac{C}{D}\right] \qquad (22)$$

For instance, the term 'A' is obtained as by substitution of all interrelated equations (5) to equation (19) and solving we obtain:

$$A = 2.86*10^{25}\mathrm{e}^{\frac{1}{\mathrm{T}}}\left[11594.20\left\{0.0000862\mathrm{T}\ln\left(1.579*10^{13}\mathrm{T}^3\left(1-0.000193\mathrm{T}-4.19*\right.\right.\right.\right.$$

$$\left.10^{-8}\mathrm{T}^2+65\mathrm{e}^{-\frac{3.62*10^{22}\left(1.519-\frac{0.00054\ \mathrm{T}^2}{\mathrm{T}+204}\right)}{\mathrm{T}}}\right)\left(\mathrm{e}^{-\frac{7.2410^{22}\left(1.519-\frac{0.00054\ \mathrm{T}^2}{\mathrm{T}+204}\right)}{\mathrm{T}}}\right)+$$

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$$\frac{25.163}{\sqrt{T^3\left(1-0.00019T-4.19*10^{-8}T^2+65e^{-\frac{3.62*10^{22}\left(1.519-\frac{0.00054\,T^2}{T+204}\right)}{T}}\right)e^{-\frac{3.62*10^{22}\left(1.519-\frac{0.00054\,T^2}{T+204}\right)}{T}}}}\Bigg) - 1.129*10^5 y +$$

$$0.00017T\ln\left[\frac{25.163}{\sqrt{T^3\left(1-0.00019T-4.19*10^{-8}T^2+65e^{-\frac{3.62*10^{22}\left(1.519-\frac{0.00054\,T^2}{T+204}\right)}{T}}\right)e^{-\frac{3.62*10^{22}\left(1.519-\frac{0.00054\,T^2}{T+204}\right)}{T}}}}\right]\Bigg\} -$$

$$0.69\Bigg] \quad (23)$$

Similar expressions are obtained for term 'B', 'C' and 'D'. Upon rigorous simplification using the values illustrated in table-1 and interrelated equations we get a simplified equation of I_{ds} which is solely dependent upon the varying temperature as

$$I_{ds} = 8.1888*10^6\,T*0.00004625*\ln[1.57929*10^{13}\,T^3(1-0.000193\,T - 4.19\,10^{-8}\,T^2)10^{-10}] \quad (24)$$

4. RESULT AND ANALYSIS

A 7nm FinFET device is simulated using Multi gate FET tool using High-k material as Lanthanum Aluminium Oxide ($LaAlO_3$) and Gallium Arsenide (GaAs) as Metal gate material using the dimensional values as illustrated in Table-1. The simulated Drain to Source Current (I_{ds}) in comparison with the analytically obtained values using Equation (24) is illustrated in Figure-3. From Figure-3 it is clear that both the simulation results and analytical results illustrate the direct relationship between the saturation current and the temperature being measured. There is a significant difference in the values obtained by simulation compared to those obtained through analysis, with the analytical values consistently higher than the simulation values. This signify that the simulation considers additional factors affecting the current, like increased scattering at higher temperatures, or in other words it indicates that the analytical model does not fully account for the complexities present in the simulation. In the analytical model, the increase in saturation current with temperature is more pronounced compared to the simulation. It is evident from the widening gap between the two lines with the rise in temperature. There appears to be a linear relationship between I_{ds} and temperature (T in kelvin) in both datasets within the temperature range displayed. It is evident that this approach will be beneficial for enhancing models, simulations, or gaining a deeper insight into the physical processes that impact the performance of FinFETs at different temperatures.

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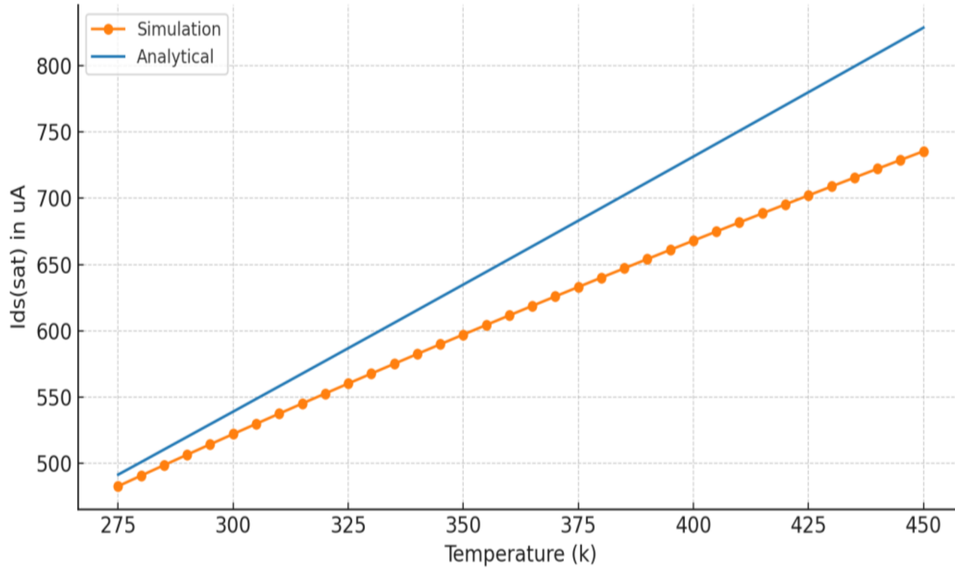

Figure 3: Analytical Model and Simulated I_{ds}(sat) Current versus Temperature variation

Temperature nanosensors are devices engineered to provide a reliable and consistent measurement of temperature. The sensitivity of a temperature sensor is its ability to accurately reflect changes in temperature, which is a critical performance metric. Semiconductor temperature sensors, like transistor based temperature nanosensors, operate based on the temperature-dependent voltage across a junction. They offer good linearity and accuracy within a moderate temperature range and are often integrated into microcontrollers and digital circuits. Describing the sensitivity of a temperature sensor often involves assessing its linearity, which indicates how the output signal changes in relation to temperature fluctuations. Understanding the information becomes simpler when using straightforward responses. It is crucial that the nanosensor accurately detects the temperature range for reliable measurements. Some specific regions within the range where certain nanosensors operate are more sensitive than others. Sensitivity can be expressed as a voltage change with temperature, often linear and specified in millivolts per Kelvin (mV/K) given by equation (25).

$$S_T = \frac{dV_{ds}}{dT} \text{ in mV/k} \quad (25)$$

From the obtained simulation results illustrated in Figure-3, the temperature sensitivity is determined and plotted in Figure-4. In semiconductor-based sensors, the bandgap energy decreases with rising temperature, influencing the rate at which carriers may be thermally stimulated. This causes a drop in current/voltage change per Kelvin (k) of temperature, resulting in a loss in sensitivity. Understanding this connection is critical in practical applications because it allows for appropriate interpretation of sensor results and calibration of temperature-dependent systems. The pattern seen in Figure 4 is typical of some kinds of temperature sensors in which the temperature-dependent parameter being monitored changes at a slower pace, even at greater temperatures. Furthermore, the data in Figure-4 reveal that the sensitivity begins slightly above 22 mV/K at the lowest temperature (about 275 K) and declines to just under 19 mV/K at the greatest temperature (approximately 450 K). Also the decline in sensitivity seems to be practically linear across the temperature range displayed, and there are no sudden shifts or anomalies in the trend, suggesting that the temperature-sensitivity connection is constant over the measured range.

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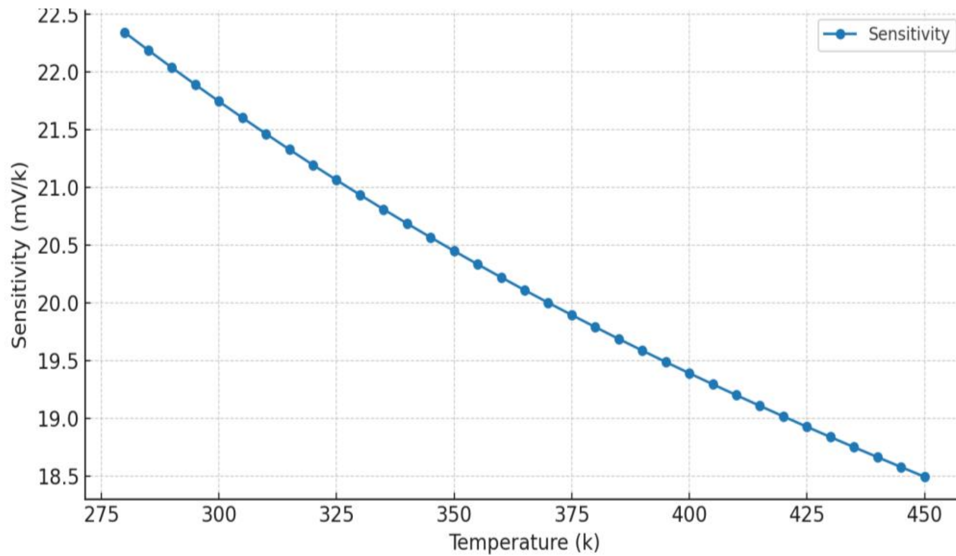

Figure 4: Measured Temperature Sensitivity versus Temperature variation

Temperature The coefficient of resistance (TCR) is defined as the relative change in resistance per degree Celsius. When the TCR is close to zero, it indicates that the material's resistance stays essentially constant throughout a wide temperature range, making it excellent for precision applications where temperature variations should have little effect on the electrical properties. For example, materials having a low or zero TCR are used in precision resistors in measurement and control systems to guarantee that measurements remain precise and constant despite temperature fluctuations. This is critical in high-precision electronics, such as those used in laboratory and industrial instruments, where temperature changes may cause inaccuracies in readings or performance. A modest TCR in semiconductors may contribute to stable electronic characteristics throughout a wide temperature range, which is important for electronic device reliability and predictability.

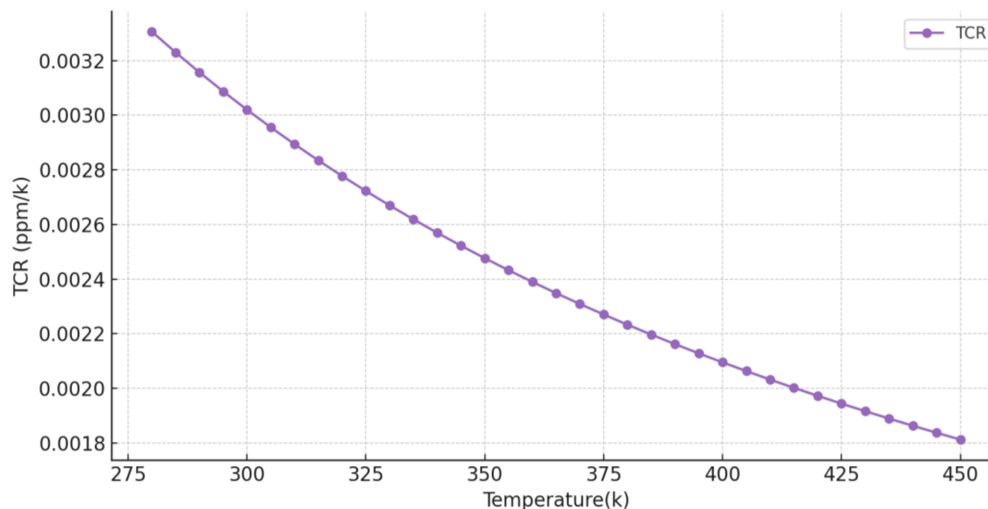

Figure 5: Measured Temperature Coefficient of Resistance (TCR) versus Temperature variation

To attain a low TCR in semiconductor materials, rigorous engineering of the material growth and device production processes is required. This excludes. This comprises carefully chosen doping concentrations and materials. In conclusion, a low TCR in semiconductors used in FETs is beneficial for ensuring stable, predictable, and dependable device operation under changing temperature

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circumstances. This feature is critical for precision electronic applications and helps to ensure the lifespan and resilience of semiconductor devices. Furthermore, it is widely known that devices may heat up significantly during operation; a low TCR aids in the prevention of thermal runaway, a phenomenon in which a rise in temperature generates further increases in power dissipation, possibly leading to device failure.

Figure-5 demonstrates a definite negative link between temperature and TCR. As the temperature rises, the TCR falls, implying that the material's resistance varies less with temperature at higher temperatures. Also The pattern seems to be linear, indicating that the TCR drops at a steady rate as temperature rises. This linear characteristic implies a predictable change in resistance across the specified temperature range. The TCR ranges from slightly over 0.0032 ppm/K at the lowest temperature (about 275 K) to below 0.0020 ppm/K at the maximum temperature (approximately 450 K). This drop in TCR with temperature is common for many materials, since the processes that cause resistance to change (such as thermal expansion and enhanced carrier scattering) may become less prominent or alter in nature as temperatures rise. The TCR's linearity over the temperature range makes it easier to develop compensating circuits or algorithms in electronic systems that must function over a large temperature range while maintaining accuracy and dependability.

5. CONCLUSION

The Drain to Source Current (Ids) model for a 7nm HK-MG FinFET is constructed using an analytical solution to Poisson's equation. Approximations in the form of assumptions are used to create a closed-form analytical model. The models developed are evaluated using a range of temperature changes in the proposed device, and their justification is demonstrated by comparing the results of simulations. Based on the result analysis, it was found that the developed models had statistically minor inaccuracies when compared to the simulation results. This is a basic model that is helpful for understanding the scalability of FinFET. Moreover, the device has an impact on the effects of heat carriers. When a nanosensor is required to retain a constant degree of sensitivity throughout a large temperature range, this feature is considered in order to ensure correct calibration within the sensor design. When it comes to designing, selecting, and using materials in temperature-critical settings, a solid grasp of the TCR and its exact definition is essential.

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